REV 1.12

Interface Description

iTrax02 GPS Receiver

This document describes the mechanical and electrical interfaces of the iTrax02 GPS receiver module.

December 11, 2002

Fastrax Ltd.

www.fastrax.fi

FastraX

CHANGE LOG

Rev.	Notes	Date
1.0	First Draft	04-07-2000
1.1	Mechanical drawings added	28-09-2000
1.2	Update due to iTrax02 rev. B	12-12-2000
1.3	Update	14-02-2001
1.4	Update, corrections	03-05-2001
1.5	Update: new RF chip, GPIO keeper	23-08-2001
1.6	Corrections, system connector pin #	27-08-2001
1.7	Update of technical specifications	19-12-2001
1.8	Application note added	25-02-2002
1.9	Update, corrections	26-07-2002
1.10	Update: corrections on application notes, added notes on LO-leakage, updates related to firmware	09-12-2002
1.11	Layout changes	10-12-2002
1.12	Technical Specification updated	11-12-2002

CONTENTS

COMPLEMENTARY READING

The following reference documents are complementary reading for this document:

Ref. #	File name	Document name
(1)		25LC640 64kbit SPI-bus Serial EEPROM Datasheet. DS21223C, Microchip.
(2)	NMEA.pdf	NMEA Protocol, Fastrax Ltd
(3)	iTalk.pdf	iTalk Protocol Specification, Fastrax Ltd

1. SYSTEM DESCRIPTION

1.1 General Description

A complete GPS receiver is implemented on the iTRAX02 module. The module includes the following features:

- 26x26mm form factor
- External, regulated +2.7...+3.3V supply
- 40-pin system connector (AMP 4-353515-0)
- Input for Active GPS antenna bias supply
- 16.3676MHz TCXO
- GPS radio based on uN8021 RF chip
- GPS base-band processor based on uN8031 chip
- Dual UART (3V CMOS levels) for serial data
- SPI-interface
- 16-bit GPIO interface
- 1PPS output signal (3V CMOS levels)
- Pulse measurement inputs (2x)
- 32768Hz RTC
- 8Mbit FLASH memory (512kx16bit)

The receiver needs only the following external inputs:

- Two separate regulated +2.7...+3.3V supplies
- Active GPS antenna bias supply (if needed)
- External reset input
- GPS Antenna signal (passive or active antenna)

Physical specification

- Size: 25.9 x 25.9 x 4.6 mm [W x L x H]

- Weight: 4 g
- Operating Temperature: -40 ºC to +85 ºC
- Operating Humidity: 0% to 95% RH, non condensing
- Vibration 4 G

Technical specification (with BOM rev. 20020521 onwards)

- Receiver: L1, C/A code
- Channels: 12
- Update rate: 1 Hz or user configurable
- AGC Range: 0…+32dB external gain
- Power supply: +2.7...+3.3V, two separate regulated power supplies for VRF and VBB
- Recommended Supply: VBB +2.8V, VRF +2.8V
- Power Consumption: *Navigating:* 130mW @ 2.7V ave.
  Idle mode (Navigation stopped): 22mW @ 2.7V typ.
  Sleep mode: 120µW @ 2.7V typ.
- Protocols: NMEA-0183 V3.0, proprietary iTALK binary protocol

Block diagram

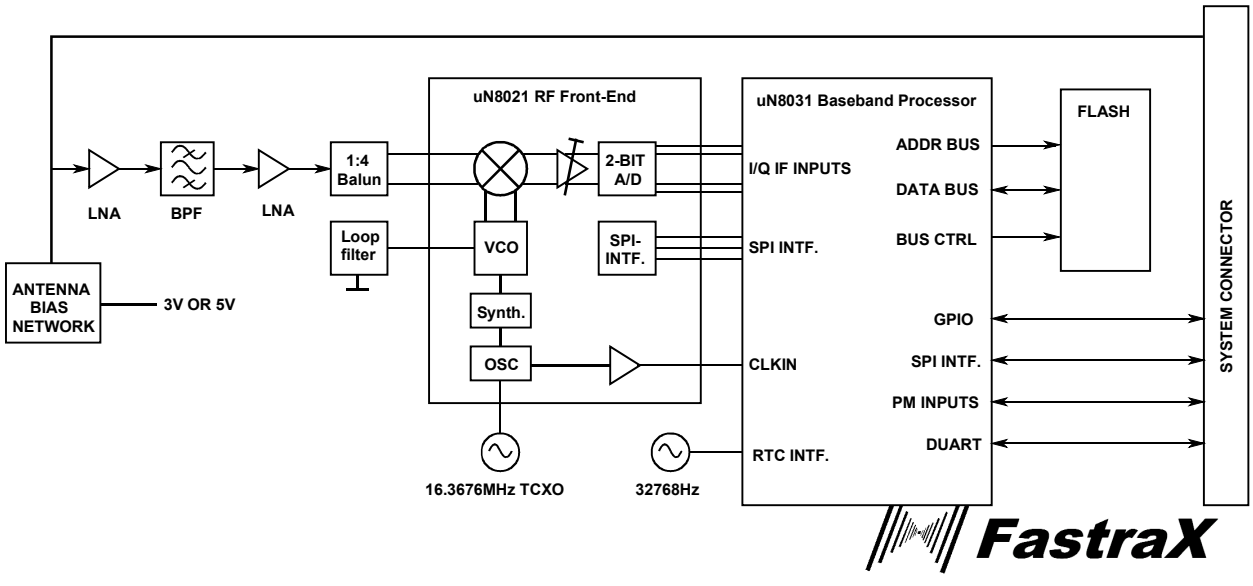


Figure 1 Block diagram of iTRAX02 GPS receiver

2. MECHANICAL SPECIFICATION

Pictures

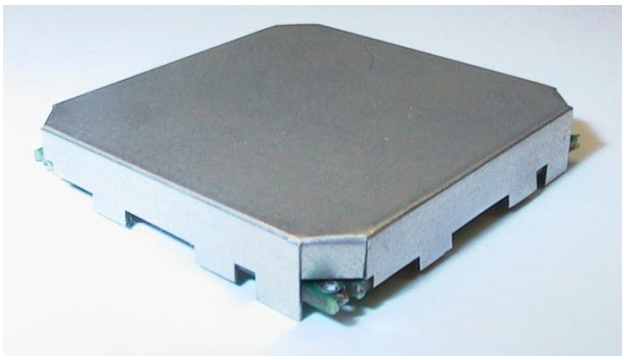


Figure 2 iTRAX02 module w/ shield

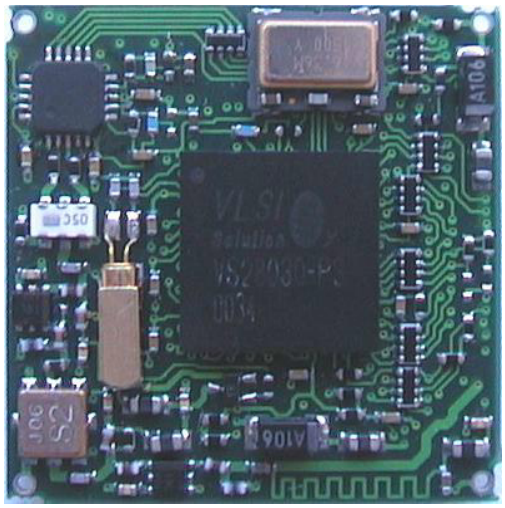


Figure 3 iTRAX02, Top view w/o shield

Figure 4 iTRAX02, Bottom view w/o shield

ITRAX02 physical dimensions

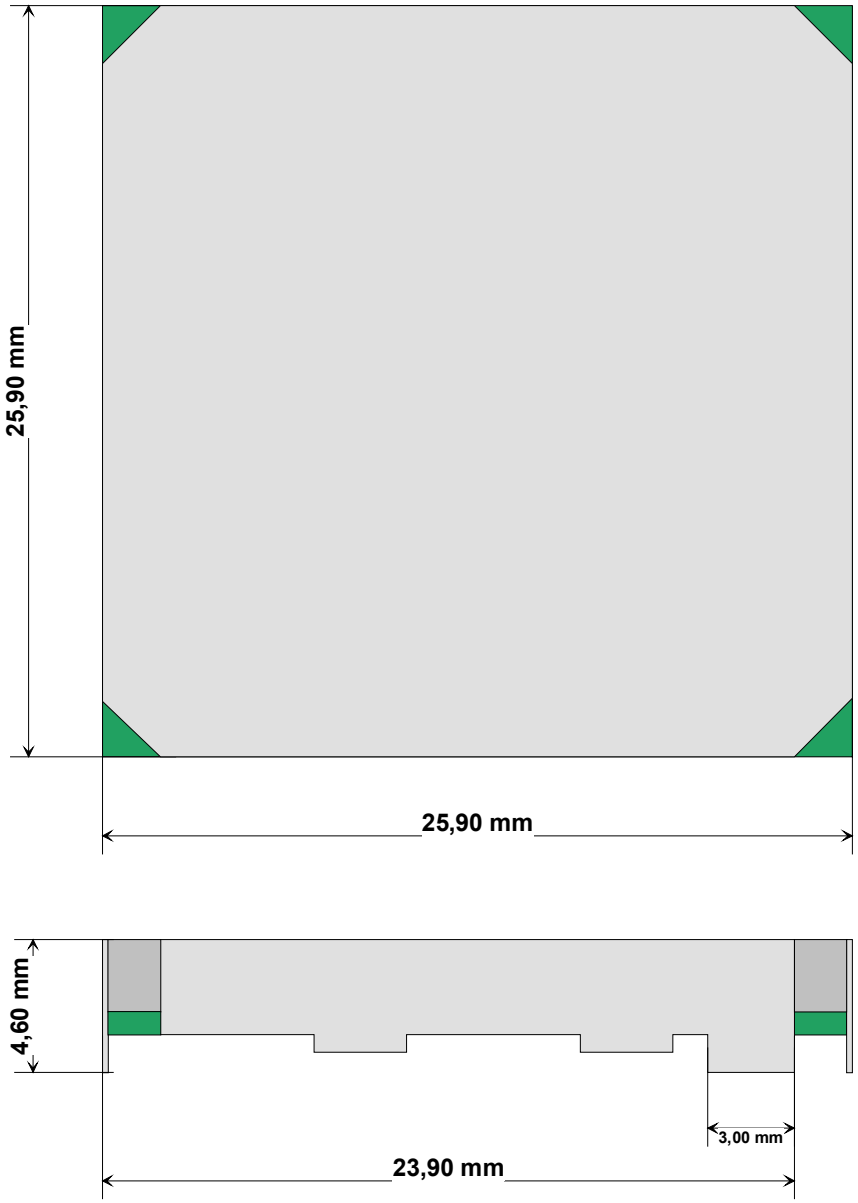


Figure 5 Physical dimensions, top and side view

Recommended PCB footprint

The figure below shows the coordinates and dimensions (in mm) of the recommended solder pads for ground (GND) and pin 1 of the mating connector. The numbers show the coordinates to the center of the pads.

It is recommended that a silkscreen printout (as shown in the figure below) is included on the PCB for ease of coordination when assembling the iTRAX02 module on the customers PCB.

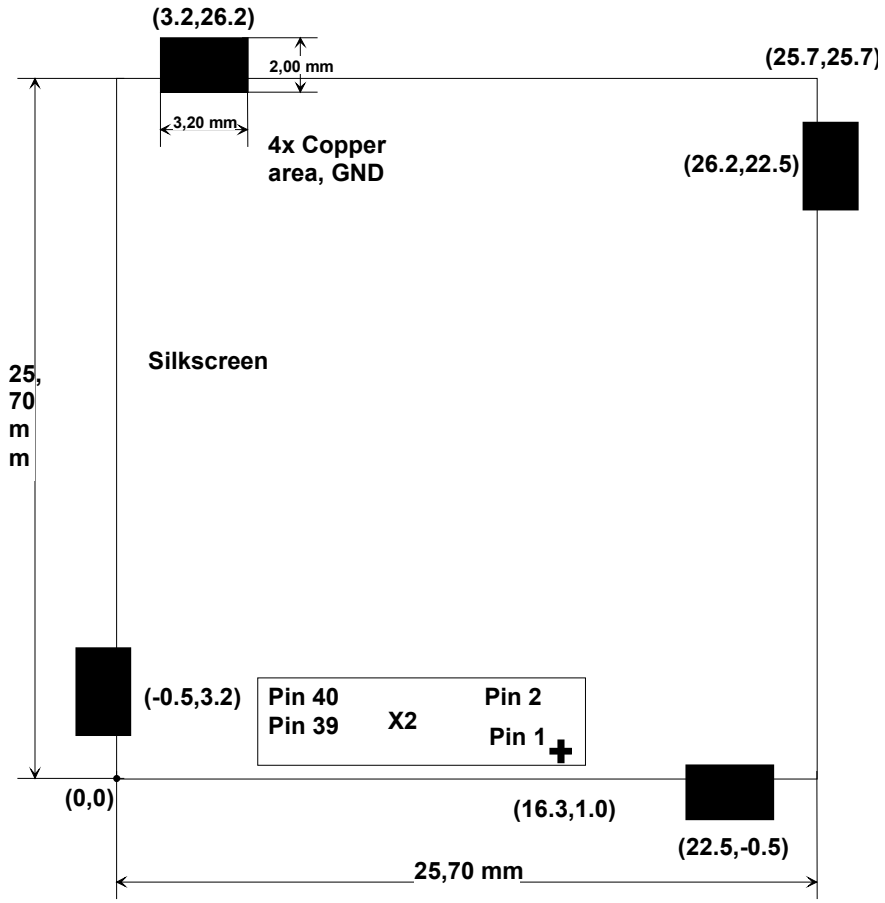


Figure 6 Recommended PCB footprint and silkscreen

It is also recommended that a solid GND plane be used below the iTRAX02 module on the customer's PCB to reduce the LO-leakage on 1575.38 MHz. This is essential when the GPS antenna is close (<0.2m) to the module, otherwise the performance may be reduced.

3. EXTERNAL INTERFACES

System connector

A 40-pin system connector, X2 (2x20 pin, 0.50mm pitch AMP connector 4-353515-0) is available for external interfacing the iTRAX02 board.

A suitable mating connector is AMP 4-353512-0 (see Appendix); samples are available from Fastrax Ltd.

The following signals are connected to X2:

▪ RF	RF input	A
▪ GPIO[0..15]	GPIO-lines	I/O
▪ PM[0..1]	Pulse measurement inputs	I
▪ SPI-bus	SPI-interface excluding SPI_XCS1	I/O
▪ UART ports	PORT0 and PORT1 UART ports	I/O
▪ PPS	PPS output signal	O
▪ XRESET	External reset (active low)	I
▪ VRF	Supply voltage for RF section	S
▪ VBB	Supply voltage for baseband section	S
▪ V_ANTENNA	External antenna bias	S

The I/O signals at the system connector are connected to uN8031 through 220ohm serial resistors.

Table 1 System connector

Pin	Signal Name	In/Out	Description (note #)
1	GPIO0	I/O	General Purpose I/O (1)
2	GPIO1	I/O	General Purpose I/O (1)
3	GPIO2	I/O	General Purpose I/O (1)
4	GPIO3	I/O	General Purpose I/O (1)
5	GPIO4	I/O	General Purpose I/O (1)
6	GPIO5	I/O	General Purpose I/O (1)
7	GPIO6	I/O	General Purpose I/O (1)
8	GPIO7	I/O	General Purpose I/O (1)
9	GPIO8	I/O	General Purpose I/O (1)
10	GPIO9	I/O	General Purpose I/O (1)
11	GPIO10	I/O	General Purpose I/O (1)
12	GPIO11	I	External Wake-up (1)
13	GPIO12	O	Int. reserved (FLASH READY/BUSY)
14	GPIO13	O	LNA control (0:LNA ON, 1:LNA OFF)
15	GPIO14	I	Boot Mode select, 1:UART, 0:SPI (3)
16	GND	Ground	Power and signal ground
17	GPIO15	I	Boot Mode select, 1:FLASH, 0:UART/SPI (3)
18	GND	Ground	Power and signal ground
19	PM0	I	Pulse Measurement Input 0 (2)
20	PM1	I	Pulse Measurement Input 1 (2)
21	SPI_SDI	I	SPI Interface Data In (6)
22	SPI_SDO	O	SPI Interface Data Out
23	SPI_SCK	O	SPI Interface Clock Out
24	SPI_XCS0	O	SPI Interface Chip Select 0 Out
25	RXD0	I	UART Port 0, Receive Data (4)
26	TXD0	O	UART Port 0, Transmit Data
27	RXD1	I	UART Port 1, Receive Data (4)
28	TXD1	O	UART Port 1, Transmit Data
29	VBB	Supply	2.7V to 3.3V Regulated DC Power Supply
30	PPS	O	1PPS signal output
31	XRESET	I	External Reset, Active Low (5)
32	GND	Ground	Power and signal ground
33	VRF	Supply	2.7V to 3.3V Regulated DC Power Supply
34	GND	Ground	Power and signal ground
35	GND	Ground	Power and signal ground
36	GND	Ground	Power and signal ground
37	RF	Analog	RF input, 50 ohm & Antenna bias ouput
38	V_ANTENNA	Supply	Antenna Bias DC Power Supply
39	GND	Ground	Power and signal ground
40	GND	Ground	Power and signal ground

Notes:

(1): The base-band processor uN8031 includes a keeper so that no external pull down or pull up resistor is needed. VIH min = 0.7 x VBB, VIL max = 0.3 x VBB. When the GPIO is configured as an input (e.g. External

Wake-up GPIO11), the drive impedance should be less than 10kohm in order to change the state.

(2): The base-band processor uN8031 includes a keeper so that no external pull down or pull up resistor is needed. VIH min = 0.7 x VBB, VIL max = 0.3 x VBB.

(3): iTRAX02 module contains internal 100k pull up resistor to VCC. VIH min = 0.7 x VCC, VIL max = 0.3 x VCC. The base-band processor uN8031 includes also a keeper and the drive impedance should be less than 10kohm in order to change the state.

(4): The base-band processor uN8031 includes an internal 100k pull up resistor to VCC (no keeper). VIH min = 0.7 x VCC, VIL max = 0.3 x VCC.

(5): iTRAX02 module contains internal 10k pull up resistor to VCC. VIH min = 0.7 x VCC, VIL max = 0.3 x VCC.

(6): The base-band processor uN8031 includes an internal 10k pull up resistor to VCC (no keeper). VIH min = 0.7 x VCC, VIL max = 0.3 x VCC.

Some of the inputs of the uN8031 include a pull-up or a pull-down resistor or a keeper; therefore external resistors to the iTRAX02 are not required. Unused pins can be left unconnected.

Power Supply

Two separate power supplies are required for VBB and VRF.

NOTE

Supply voltage for RF section (VRF) should be linearly regulated and it should be with low ripple (<2 mVp-p). Do not use the same supply voltage from a single regulator for VRF and VBB since the RF section gets interference from the VBB ripple.

The power supply should be able to supply up to 50mA current peaks for both VBB and VRF.

Reset

NOTE

iTRAX02 requires an external Power-On-Reset (POR) circuit which provides a reset pulse at XRESET-pin after the supply voltages are connected. The reset pulse should be active (low state) at least 100ms after power-up.

SPI-interface

The SPI-compatible interface is used for the following purposes:

- Optional external EEPROM memory (e.g. 25LC640)
- Active control of uN8021 RF chip

The SPI peripherals have separate Chip Select signals. The data signals are common. The SPI signals are also routed to system connector X2 (except for SPI_XCS1).

The SPI signals are utilized the following way:

- Out SPI_SDO: SPI Data Out
- Out: SPI_SCK: SPI Data Clock Out
- In: SPI_SDI: SPI Data In
- Out SPI_XCS0: Optional external EEPROM memory
- Out SPI_XCS1: reserved for uN8021 RF chip

UN8031 is always the master and all SPI-compatible peripherals are slaves.

Note that the SPI-interface looks like a memory interface i.e. the SPI interface clocks out op-codes and commands prior to actual data required for accessing e.g. EEPROM memory, see figure below. This must be handled with SW on the slave side. Further details can be found e.g. in reference (1).

The uN8021 RF chip includes a ‘memory compatible’ SPI-interface.

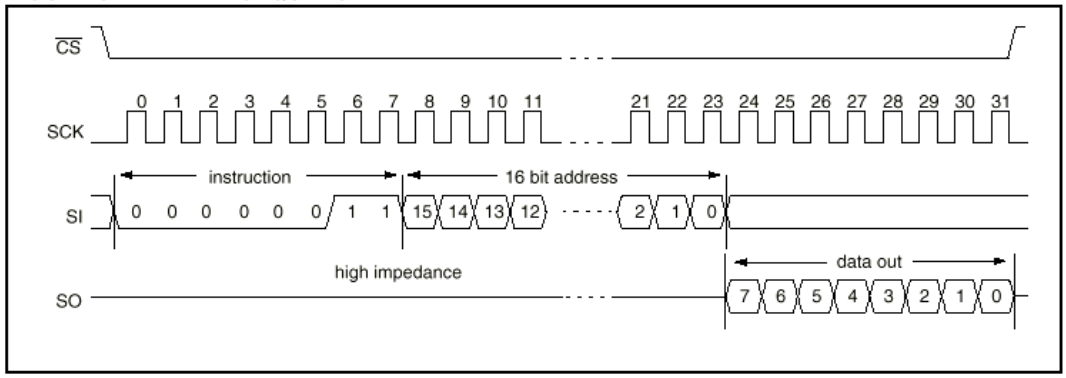


Figure 7 Example of SPI interface usage, EEPROM read sequence

UART interface

Two asynchronous UART ports are available for serial interfacing. The baud rates are fully programmable. See reference (2, 3) for more details.

The data format is however fixed: x,N,8,1, i.e. x baud, No parity, eight data bits and 1 stop bit. No other data formats are supported. LSB is sent first. CMOS signal levels are used.

Start	D0	D1	D2	D3	D4	D5	D6	D7	Stop

Parity: N
Data Bits: 8
Stop bits: 1

Figure 8 UART Data format.

The UART ports are named PORT0 and PORT1. PORT0 is used e.g. for booting. PORT1 can be utilized for the emulator or NMEA interface.

GPIO interface

A 16-bit GPIO port is available for external interfaces. Each of the GPIO-lines can be programmed for generating interrupts. Two of the GPIO-lines (GPIO14 and GPIO15) are reserved for Boot Mode Select as described below.

Table 2 Boot mode select

GPIO15	GPIO14	Boot Mode
0	0	Boot from EEPROM memory through SPI-port
0	1	Boot through UART PORT0 at 115200baud
1	x	Boot from flash

The iTRAX02 is configured for booting from Flash memory as a default. This is achieved with the internal pull-up resistors R12 and R13 at GPIO14&15. Other boot modes can be selected with external drive at the system connector (i.e. in Evaluation Kit, or by external host) at GPIO14&15.

One of the GPIO-lines (GPIO13) is reserved for active power control of the internal LNA and it can be also used for controlling external LNA. Also GPIO12 is reserved internally for controlling the flash memory.

GPIO11 is reserved for external Wake-up after setting iTRAX02 to sleep state, see complementary reading (2) or (3). The GPIO11 detects a transition from state 1->0 or from 0->1 as a Wake-up command.

NOTE

When the GPIO is configured as an input (e.g. GPIO11, 14 and 15), the keeper on the base-band processor uN8031 needs less than 10kohm drive impedance in order to change the input state.

PM-interface

The iTRAX02 has two pulse measurement devices, which can be used to measure with great accuracy how long an input stays high or low. The pulse measurement devices support several accuracy modes, trigger modes (once-only, continuous wait and continuous) and input inversion.

NOTE

The keeper on the base-band processor uN8031 needs less than 10kohm drive impedance in order to change the PM input state.

RF-interface

An external GPS antenna (active or passive) can be connected to the iTRAX02 using the RF-input line at connector X2. A 50 ohm PCB stripline is needed on the motherboard, see figure below for example layout.

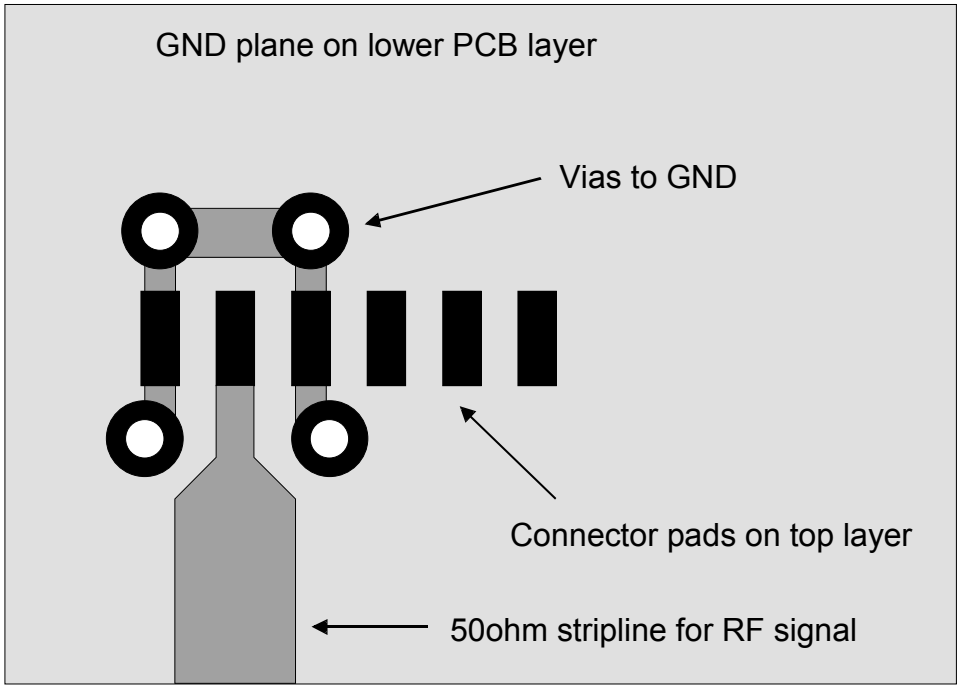


Figure 9 Example of RF interface layout on customer PCB

The width of the 50ohm stripline is dependent of the PCB material and thickness. On FR4 material the width [W] (at 1.5GHz) is roughly 2 times the thickness [H] of the PCB. If the PCB thickness is for example 0.8mm then the width of the stripline should be 1.6mm and so on.

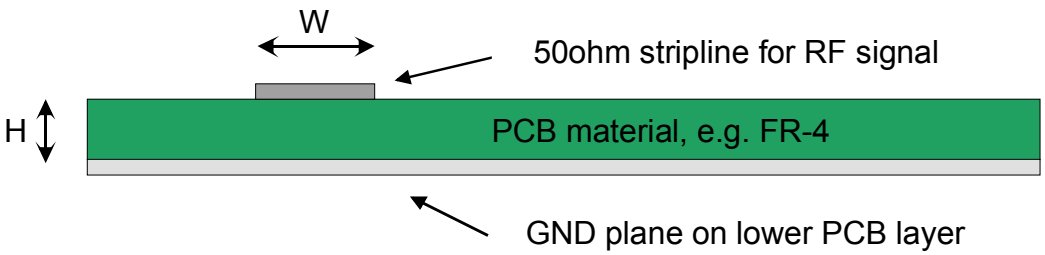


Figure 10 Stripline width versus PCB thickness

The antenna bias for an external active antenna can be provided through the V_ANTENNA input found on the X2 system connector. The V_ANTENNA voltage should be chosen according to the antenna to be used.

NOTE

Maximum supply current for V_ANTENNA should be externally limited to 100mA.

The internal bias network is formed by a stripline, ferrite coil and coupling capacitor, which are used for passing the antenna bias voltage to the RF-input.

Interfacing considerations

The following recommendations should be taken into account when interfacing to the iTRAX02 GPS receiver:

- The iTRAX02 can be used with passive antennas if the cable loss is below 1 dB. Otherwise an active antenna is needed to compensate for the cable loss. Net gain from the active antenna prior iTRAX02 should be between 6 and 32 dB.

- Use a solid GND plane under the iTRAX02 module to reduce LO-leakage at 1575 MHz, especially when the GPS antenna is close (<0.2 m) to the module. Use also 18 pF (0402) shunt capacitors close to the system connector to reduce risk for LO-leakage.

- AGC range is 32 dB, which means that for iTRAX02 module the external gain at 1575 MHz should not exceed 32 dB.

- Due to the high external gain strong out-of-band signals may block the front-end. Blocking level is about –2 dBm at the RF input @ S/N degradation 3 dB.

The receiver has a zero-IF topology. If two receivers are connected to the same antenna, the local oscillator leakage may cause blocking. Use a power combiner/splitter that gives at least 20 dB isolation between ports.

4. APPLICATION NOTES FOR ITRAX02

External Interfaces

This section describes a recommended interface for the iTRAX02 receiver.

The minimum set of external interfaces are:

- Power supply
- RF input
- External Reset

Additionally there are some useful interfaces:

- Boot Mode Select using GPIO15 (dedicated GPIO pin)
- Control of external antenna bias through GPIO13 (dedicated GPIO pin)
- External Wake-up control using GPIO11 (dedicated GPIO pin)

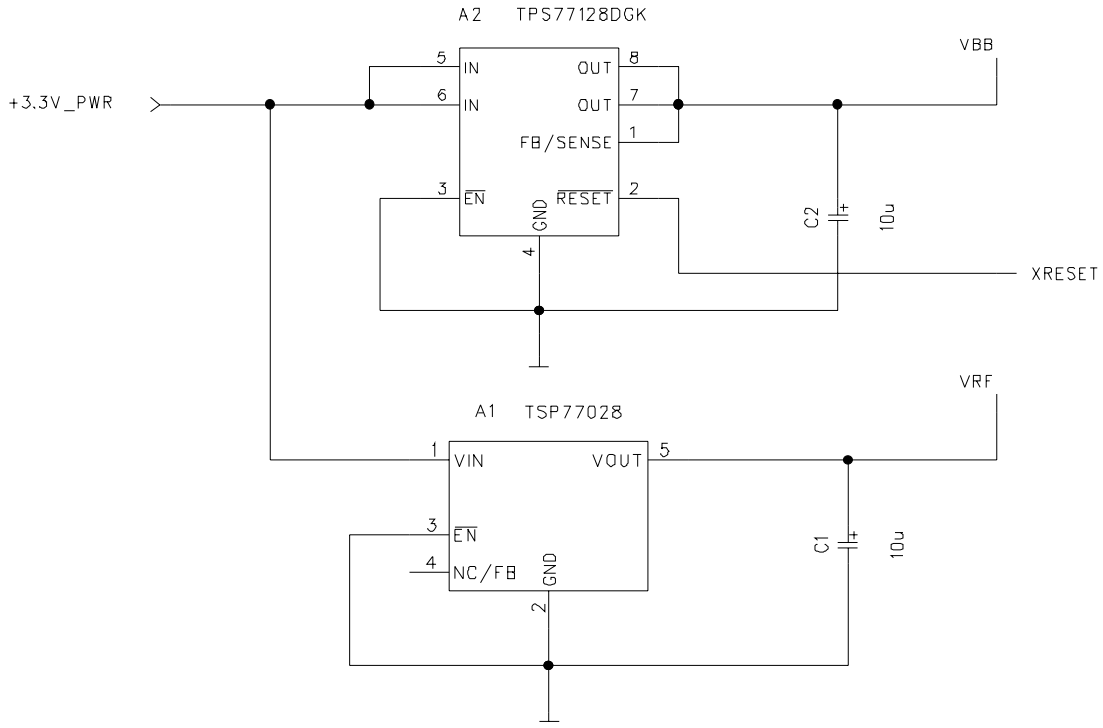
Note that GPIO14 and GPIO12 are also dedicated GPIO pins and are thus not available for the customer.

Rest of the I/O is also available for customer applications.

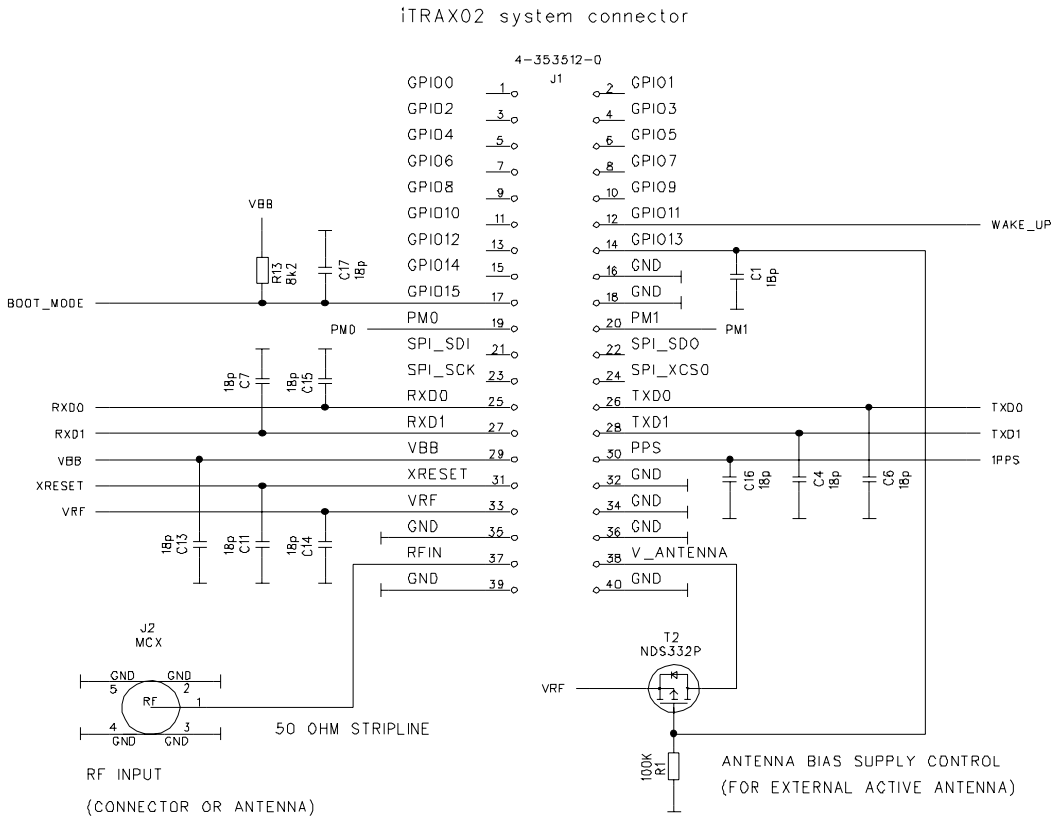
Power Supply

Two separate power supplies must be used for VRF and VBB. A suggested power regulation is shown in the picture below. The TPS77127DGK from Texas Instruments provides also a reset pulse with 220ms delay for the iTRAX02 module.

Power regulation



Interface signals



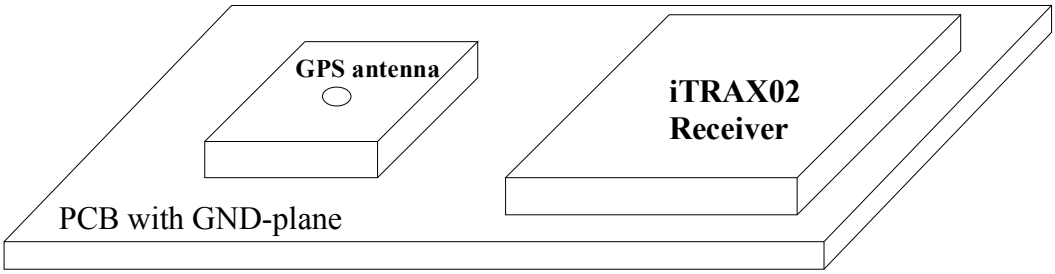
Some of the GPIO are reserved internally for iTRAX02 (see section 4.4).

There is a support in the iTRAX02 firmware for control of an active antenna bias. The GPIO13 can be used to control an external switch or regulator. See the reference application in the schematic picture above.

Note the usage of 18pF shunt capacitors to reduce risk for LO-leakage at 1575MHz, which may reduce the performance. Use also a solid GND plane under the iTRAX02 module, especially when the GPS antenna is close to the module.

Antenna issues

The iTRAX02 GPS receiver can be used with a passive antenna. One typical application is shown below where the GPS antenna and the receiver are adjacent on the same side of the PCB.



In case a patch antenna element is used the user must take into account a few factors that effects antenna performance:

- Size of patch element: smaller elements tend to give lower signal levels due to reduced radiation efficiency.

- Size of GND plane under the patch element: smaller than 70mm GND plane reduces antenna directivity and signal levels.

- Avoid unsymmetrical GND plane: polarization characteristics declines causing polarization miss match loss (reduction in signal levels) and reduction in multi path mitigation (navigation accuracy).

These all issues affect the radiation pattern and the resonance frequency of the antenna. The antenna selection and design is a very critical issue and must be reviewed case-by-case. Please consult Fastrax regarding antenna implementation.

Note also that the enclosure material (e.g. plastic cover) also affect the resonance frequency in such a way that plastic material close to the antenna element move the resonance frequency downwards. This must be taken also into consideration when specifying the antenna resonance frequency.

5. APPENDIX

Mating system connector 40-pin AMP 4-353512-0

AMP

Fine Pitch SMT Stacking Connectors
(Parallel Board-to-Board)

Catalog
889092
Revised 2-99

0.5mm Fine Stack Receptacles, 0.5 [.020] Pitch

1.5 [.059] Stacking Height

Material and Finish:

Housing — 6T nylon, high heat resistant resin

Contacts — Phosphor bronze, plated AMP-DURAGOLD with entire contact underplated nickel

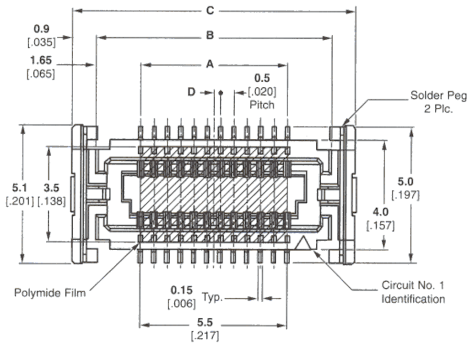
Solder Pegs — Copper alloy, plated tin-lead

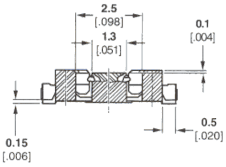
Related Product Data:

Mating Tabs — page 9

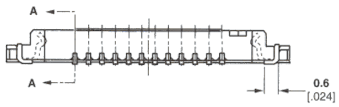
Technical Documents (Page 70):

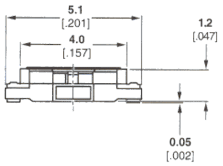
AMP Product Specification
108-5546

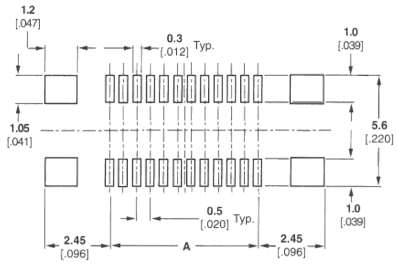




Section A - A







Recommended PC Board Layout
(PC Board Thickness = 0.6 [.024] Min.)

No. of Positions	Dimensions A	B	C	D	Keyed	Receptacle Part Numbers
20	4.5 .177	7.8 .307	9.6 .378	0.25 .010	Yes	2-353512-0
30	7.0 .276	10.3 .406	12.1 .476	0.0	Yes	3-353512-0
40	9.5 .374	12.8 .504	14.6 .575	0.25 .010	Yes	4-353512-0
50	12.0 .472	15.3 .602	17.1 .673	0.0	No	5-353159-0
60	14.5 .571	17.8 .701	19.6 .772	0.25 .010	No	6-353159-0
70	17.0 .669	20.3 .799	22.1 .870	0.0	No	7-353159-0
80	19.5 .768	22.8 .898	24.6 .969	0.25 .010	No	8-353159-0

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www.amp.com | 1-800-522-6752 Product Information Center/AMP FAX Service | 1-800-722-1111 Tooling/Technical Assistance Center | Specifications subject to change